PATENT
P54266

Brief (3)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Geun-Woo PARK

Serial No.: 08/922,300 Examiner: M. Marc-Coleman

Filed: 2 September 1997 Art Unit: 3661

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

Appeal No._____

The Honorable Commissioner
of Patents & Trademarks
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 CFR §1.192)

This brief is in furtherance of the Notice of Appeal filed in this case on 12 June 2001.

The fees required under §1.17(f) for the filing of the Appellant's Brief are dealt with in the accompanying transmittal letter.

This brief is transmitted in triplicate (37 CFR §1.192(a)).

APPEAL BRIEF

I. STATEMENT OF REAL PARTY IN INTEREST

Pursuant to 37 CFR §1.192(c)(1) the real party in interest is:

SamSung Electronics Co., Ltd.
416 Maetan-dong, Paldal-ku,
Suwon City, Kyungki-do,
Republic of Korea

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 CFR §1.192(c)(2), there are no appeals nor interferences known to the Appellant, the Appellant's legal representative, or the Assignee (real party of interest) which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-11 have been finally rejected and are appealed herein.

IV. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendment has been filed after receipt of the final rejection (Paper No. 17).

V. SUMMARY OF THE INVENTION

Page 10, line 5 - Page 13, line 11

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a

power interruption delay function in accordance with the present invention. In the display device of Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result,

the H/V processor constant voltage circuit 131 does not immediately stop the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant

voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power supply is resumed after power interruption. Further, the power interruption delay charging circuit can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

VI. ISSUES

Whether claims 1-11 are patentable under 35 U.S.C. §103(a) over Applicant's admitted prior art in view of Van Clifton.

VII. GROUPING OF CLAIMS

Claim 1 stands or falls alone, and claims 2-11 stand or fall with claim 1.

VIII. ARGUMENT

Claims 1-11 are not obvious and unpatentable under 35 U.S.C. §103(a) in view of the combined teachings of Applicant's admitted prior art and Van Clifton Martin '348 (*hereafter:* Martin). The Applicant respectfully traverses this rejection for the following reason(s).

With respect to claim 1, Applicant's admitted prior art teaches all that is claimed except the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted,* which is deemed to be non-obvious in view of the proposed combination of art.

Similarly, claim 3 calls for *power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted*; and claim 8 calls for *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.* Accordingly, the argument traversing the §103 rejection of claim 1 applies equally to the patentability of claims 3 and 8.

The Examiner applies Martin in an erroneous attempt to obviate the claims. The Examiner refers us to col. 2, lines 64-72, which state:

> The control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed.

Martin fails to teach or suggest, to one of ordinary skill in the art, gradually lowering the input voltage to a H/V processor constant voltage circuit when power supplied to the display device is interrupted.

Instead Martin would have suggested **only** what Martin teaches, *i.e.*, clamping a control grid (not shown) of the monitor of Applicant's admitted prior art to a negative DC bias voltage -V1 from a power supply by a diode connected between voltage -V1 and the control grid and a capacitor connected between the control grid and ground.

It is well known in the art that control grid 14 in Martin's CRT(cathode ray tube) is not the

same as a deflection yoke of a CRT. It is also well known that the bias voltage applied to a control grid does not have the same function as the horizontal and vertical synchronizing signals applied to the deflection yoke. It is further well known in the art that **a H/V processor constant voltage circuit** (claims 1 and 8) or a **horizontal deflection circuit** (claim 3) does not provide the bias voltage applied to a control grid of a CRT.

Accordingly, the application of the protection circuit, *i.e.,* diode 44 and capacitor 45 in Martin, for making the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed, is absolutely different than that claimed in claim 1, *power interruption delay charging means* ***for gradually lowering said input voltage to said H/V processor constant voltage circuit*** *when power supplied to said display device is interrupted* (emphasis added).

The Examiner has the burden to show some teaching or suggestion in the references to support their use in the particular claimed combination. The Examiner's only explanation of how or why one of ordinary skill in the art would have been motivated to apply diode 44 and capacitor 45 of Martin **to the input of H/V processor constant voltage circuit** of Applicant's admitted prior art is so "that the CRT display would be protected in case of sudden failure." Martin does not discuss a **H/V processor constant voltage circuit** and thus does not address the issue of **gradually lowering an input voltage to a H/V processor constant voltage circuit** "in case of sudden failure." Accordingly, Martin fails to teach *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.* Additionally, Applicant's admitted prior art also fails to address the issue of **gradually lowering an input voltage to a H/V processor constant voltage circuit** "in case of sudden failure." Therefore, the combined teachings of Applicant's admitted prior art and Martin

fails to teach *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.*

As noted above, Martin only teaches, slowly dropping the voltage at the **control grid** 14 of the monitor, thus if one of ordinary skill in the art was motivated my Martin to modify a monitor of the Applicant's admitted prior art, such a modification would only entail slowly dropping the voltage at the **control grid**. This is in no way similar to *gradually lowering said input voltage to said H/V processor constant voltage circuit* as set forth in claim 1. *In re Rijckaert*, 28 USPQ2d 1955 (CAFC 1993) states:

> "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell,* 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rhinehart,* 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Accordingly, the rejection of claims 1-11 is deemed to be in error and should not be sustained.

IX. SUMMARY

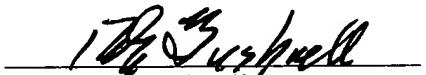
As can be determined from the foregoing arguments, the issue is not one of "motivation to combine" (see page 9 of Paper No. 17), but is instead one of whether the claim, as a whole, is taught by the combined prior art. Since the applied art fails to teach the **whole** feature of *power interruption **delay charging means** for **gradually lowering said input voltage to said H/V processor***

constant voltage circuit *when power supplied to said display device is interrupted,* then the rejection is in error.

It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art. *In re Wesslau,* 353 F.2d 238, 241, 147 USPQ 391, 393 (CCPA 1965); see also *In re Mercer*, 515 F.2d 1161, 1165-66, 185 USPQ 774, 778 (CCPA 1975).

Accordingly, the rejection of claims 1-11 is deemed to be in error and should not be sustained.

Respectfully submitted,



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X. APPENDIX

CLAIMS UNDER APPEAL

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said

H/V processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial AC power into a DC input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said DC input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged

on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to said DC input voltage, said DC input voltage being received through said power interruption delay charging means.

5. The display device as set forth in claim 4, wherein said current amplifier comprises:

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor FET1 having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to said ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal.

6. The display device as set forth in claim 5, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

7. The display device as set forth in claim 6, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.

8. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to a ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

9. The display device as set forth in claim 8, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

10. The display device as set forth in claim 8, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

11. The display device as set forth in claim 10, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.